PROJECT ABSTRACT

Overcurrent Relay Coordination Demonstration Panel

A bench demonstration panel with two inverse-time overcurrent relay stages (IDMT) that shows protection grading and coordination: fault injection at two points, a fast downstream trip, a delayed upstream backup trip, and an LCD displaying each stage's trip time in milliseconds. The entire rig runs on extra-low-voltage DC, safe for classroom demonstration.

Project type: Hardware

Availability: Built to order

Suitable branch: Electrical

Technologies: Arduino Uno, IDMT overcurrent logic, ACS712 current sensors, IEC 60255-151 curve, 12 V DC lamp loads, 16x2 LCD display, relay driver modules, terminal block wiring

Price: Request a quotation

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1. Title

Overcurrent Relay Coordination Demonstration Panel — a bench panel with two inverse-time overcurrent relay stages (IDMT) that demonstrates protection grading and coordination through fault injection at two points, with trip times displayed in milliseconds.

2. Introduction / Background

In a distribution network, protection relays are arranged in series and must be graded so that the relay nearest a fault trips first while upstream relays wait as delayed backup — the principle of selectivity. Inverse definite minimum time (IDMT) overcurrent relays implement this through current-dependent operating times defined by standard curves such as IEC 60255-151. Students usually meet these ideas only as textbook formulas; commercial relay test sets that could demonstrate them cost far more than a college laboratory can justify. This project provides an affordable bench alternative: a two-stage IDMT demonstration panel built on a microcontroller, running entirely on extra-low-voltage DC, that makes grading and backup protection visible as a sequence of trips and times.

3. Problem Statement

Protection grading is one of the most important and least demonstrable concepts in undergraduate power-system courses. Textbook treatment reduces it to curve-plotting exercises, while real relay test equipment is prohibitively expensive for most teaching laboratories. As a result, students complete the topic without ever watching selectivity happen — a fast downstream trip, an upstream stage that starts but resets, and a backup trip for a fault beyond the downstream stage's reach. There is a need for a safe, low-cost bench rig that turns the grading margin from a calculated number into a visible, repeatable demonstration.

4. Objectives

- Demonstrate inverse-time overcurrent protection with two series relay stages following the IEC 60255-151 standard-inverse curve.
- Show selectivity: downstream-zone faults cleared fast by the downstream stage while the upstream stage starts but resets.
- Show backup protection: upstream-zone faults cleared by the delayed upstream stage.
- Make the time multiplier setting (TMS) and pickup configurable per stage so the grading margin can be changed and re-demonstrated.
- Display each stage's detection-to-trip time in milliseconds on an LCD for direct comparison with the calculated margin.
- Keep the entire demonstration on extra-low-voltage DC for safe classroom use.

5. Proposed Methodology

- Implement two IDMT overcurrent stages in Arduino firmware, evaluating the IEC 60255-151 standard-inverse operating time from sampled zone currents, per-stage TMS (0.1–1.0) and pickup settings.
- Sense each zone's current with ACS712 hall-effect modules; represent healthy and fault currents with 12 V lamp load banks switched by fault pushbuttons at two injection points.
- Drive trip outputs through relay modules with separate amber (TRIP D) and red (TRIP U) indicator lamps, an analog ammeter for fault current, and a 16x2 LCD latching trip times in milliseconds.
- Provide a grading calculation worksheet so the student predicts operating times and the grading margin from the configured TMS/pickup before running each fault test.
- Validate the demonstration by repeating fault injections at several TMS settings and comparing observed trip times against the curve predictions documented in the commissioning report.

6. System Architecture / Working

The panel is powered from a 12 V DC adapter with 5 V on-board regulation. A lamp load bank draws a steady healthy-load current shown on the analog ammeter. Pressing FAULT A switches a low-resistance lamp path into the downstream zone, raising the sensed current in both zones above pickup. The controller evaluates the IEC standard-inverse operating time for each stage from its TMS and pickup; the downstream stage, set with the lower TMS, reaches its operating time first (approximately 120 ms at default settings), opens its trip relay, lights TRIP D and latches the time on the LCD. The upstream stage had started timing but the fault clears before its longer operating time (approximately 280 ms) elapses, so it resets — selectivity. Pressing FAULT B injects the fault in the upstream zone beyond the downstream stage's reach, so only the delayed upstream stage trips, lighting TRIP U as backup protection. A panel RESET rearms the rig for the next test.

7. Hardware / Software Requirements

- Arduino Uno (ATmega328P) control board with IDMT firmware (C/C++).
- Two ACS712 hall-effect current sensor modules (one per zone).
- 12 V DC lamp load banks for healthy and fault currents (approximately 0.5–3 A fault range, design target).
- Relay modules for trip outputs; amber and red panel indicator lamps; two fault-injection pushbuttons; panel reset button.
- 16x2 LCD display (1 ms trip-time resolution); analog ammeter 0–5 A.
- 12 V DC adapter (approximately 2 A) with 5 V on-board regulation; terminal blocks and panel enclosure (approximately 45 × 35 cm).
- No mains connection anywhere in the demonstration circuit.

8. Expected Outcomes

- A working bench panel that visibly demonstrates protection grading: fast downstream trip, upstream reset, and delayed upstream backup trip.
- Trip times latched on the LCD per test, comparable against the IEC-curve grading worksheet (grading margin approximately 150 ms at default settings, design target).
- A repeatable fault-injection test procedure usable for classroom demonstration and viva examination.
- Complete documentation: circuit diagram, wiring schedule, grading worksheet, report PDF, PPT and viva Q&A.;

9. Applications

- Undergraduate power-system and switchgear-and-protection laboratory demonstrations.
- Classroom teaching of IDMT curves, TMS, pickup, grading margin and selectivity.

- Final-year project viva demonstration for Electrical / EEE students.
- Training aid for junior protection engineers learning coordination principles (educational, not a substitute for certified relay testing).

10. Future Scope

- Three-phase version with per-phase current sensing and a residual earth-fault stage.
- Definite-time and very/extremely-inverse curve options selectable from the panel.
- Serial/USB logging of trip events for plotting time–current coordination charts on a PC.
- Directional overcurrent element demonstration with a phase-angle reference input.
- Enclosure and graphics upgrade for permanent laboratory installation.