PROJECT ABSTRACT

Cascaded H-Bridge Multilevel Inverter (Five-Level)

Single-phase five-level cascaded H-bridge inverter prototype using two MOSFET bridges, isolated DC sources and Arduino gate control.

01. Title

Cascaded H-Bridge Multilevel Inverter (Five-Level)

02. Introduction / Background

Two-level inverters are simple but produce harmonic-rich square-ish waveforms that heat motors and distort sensitive loads. Multilevel inverters address this by synthesising the output from smaller voltage steps, forming a staircase that approximates a sine wave with far lower harmonic content and lower switching stress. The cascaded H-bridge — series-connected full-bridge cells, each on its own isolated DC source — is the classic topology for teaching the concept. This project builds a single-phase five-level cascaded H-bridge as a low-voltage laboratory prototype, with the switching sequence, isolation practice and waveform verification all visible on the bench.

03. Problem Statement

Power-electronics students usually meet multilevel inverters only as simulation waveforms. There is a need for a physical bench prototype that shows the real engineering behind the topology: why each bridge needs its own isolated DC bus, how opto-isolated gate drivers separate logic from power, what dead time does, and how the five-step staircase actually looks on a CRO next to a two-level waveform. The prototype must stay at safe low voltage while remaining faithful to the topology.

04. Objectives

- Build two MOSFET H-bridge modules whose series outputs synthesise a five-level staircase at 50 Hz.

- Provide two isolated 12 V DC sources demonstrating the floating-bus requirement of the topology.
- Implement opto-isolated gate driving with programmed dead time from an Arduino.
- Make the switching-angle table editable in firmware for selective-harmonic-elimination style experiments.
- Provide fused DC buses and CRO test points with a guided waveform-comparison demo script.

05. Proposed Methodology

The methodology has three stages. (1) Power stage: two H-bridge modules are built with power MOSFETs on heatsinks, DC-link capacitors and fusing; each is fed by its own transformer-rectifier 12 V supply so the buses float independently. (2) Control: an Arduino generates eight gate signals from an editable angle table, through opto-isolated drivers with dead time, with gate resistors and documented freewheeling paths. (3) Verification: the demo script captures the staircase on a CRO and compares it against a two-level bridge waveform on the same instrument, with an optional LC filter stage.

06. System Architecture / Working

The two isolated 12 V supplies power the two bridges independently. The Arduino computes gate timing from its switching-angle table and outputs eight logic signals; opto-isolated drivers convert these to gate drive with dead time between complementary devices. Each bridge outputs +Vdc, 0 or −Vdc, and the series connection sums them into the five-level staircase (+2Vdc, +Vdc, 0, −Vdc, −2Vdc) at 50 Hz. The staircase feeds a resistive demo lamp, optionally through an LC filter, with CRO test points at the output.

07. Hardware / Software Requirements

- Power MOSFETs with aluminium heatsinks (two H-bridge modules)
- Opto-isolated gate driver ICs with gate resistors
- Arduino Uno/Nano for switching-sequence generation
- Two isolated 12 V transformer-rectifier DC supplies with fusing
- DC-link electrolytic capacitors, resistive demo lamp, optional LC filter
- CRO/DSO for waveform capture and comparison
- Arduino IDE for the switching firmware

08. Expected Outcomes

The expected outcome is a bench prototype producing a clean five-step staircase at 50 Hz from an approximately 24 V peak DC stack, with the CRO comparison visibly showing lower harmonic content than the two-level reference. The editable angle table is expected to let students observe how switching angles reshape the steps. THD figures are not pre-claimed: harmonic content is observed by the buyer on the CRO during the demo, and the report presents the waveforms rather than invented numbers.

09. Applications

- Teaching rig for multilevel inverter topologies and harmonic analysis
- Laboratory demonstration of gate driving, isolation and dead time
- Base for selective-harmonic-elimination and SPWM switching experiments
- Viva and exhibition piece for power-electronics coursework

10. Future Scope

- Extending to seven or nine levels with additional cascaded cells
- Sinusoidal PWM and selective-harmonic-elimination switching schemes
- Closed-loop output voltage regulation with feedback
- Three-phase extension of the cascaded topology

11. References

- Rodriguez, J., Lai, J. S. and Peng, F. Z. — Multilevel inverters: a survey of topologies, controls, and applications. IEEE Transactions on Industrial Electronics, 2002.
- Mohan, N., Undeland, T. M. and Robbins, W. P. — Power Electronics: Converters, Applications, and Design. Wiley.